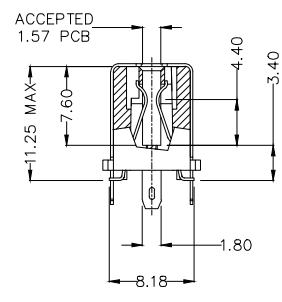
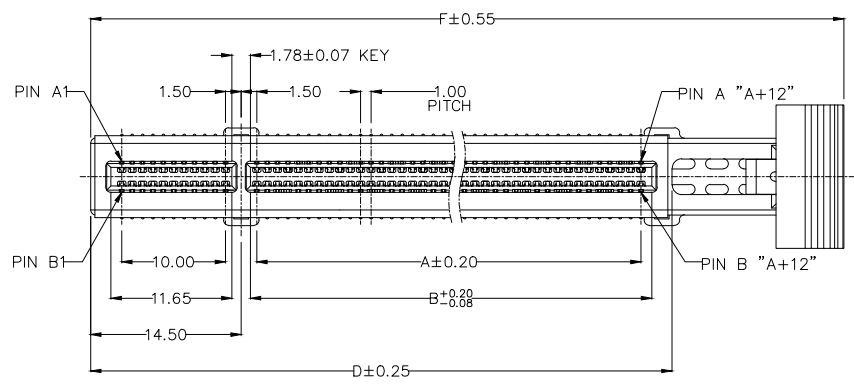


REV	LOCATIONS	DESCRIPTION	DATE	REVISER	APPD

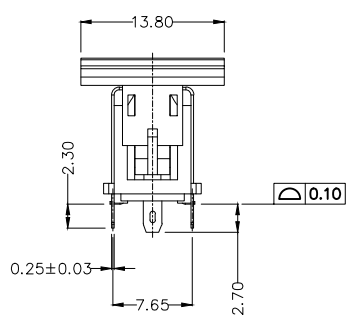
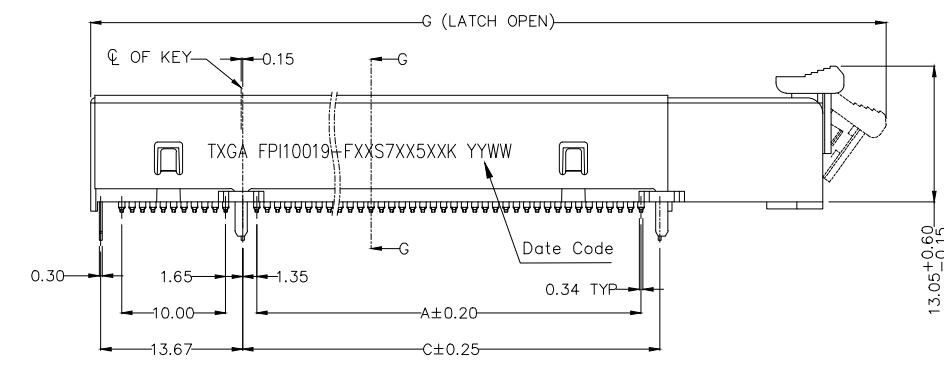


**SPECIFICATION**  
Electrical

Current Rating: 1.1A AC(rms)/DC  
Voltage Rating: 50V AC(rms)/DC  
Contact Resistance: 30 mΩ Max  
Insulation Resistance: 1000 MΩ MIN  
Withstanding Voltage: 500V AC r.m.s  
Temperature Range-Operating: -40°C~+85°C

Material

Housing: PA9T, (UL 94V-0)  
Contact: Copper Alloy/, Selective gold plated on contact area and matte tin plated on tails area  
Tab: Copper Alloy/100u" Min. matte Tin Plated  
Shell: SUS/100u" Min. Matte-Tin Plating on the Soldering Area



**Ordering Information**

FPI 100 19 — F XX S 7 XX 5 XX K  
1 2 3 4 5 6 7 8 9 10 11

1 Category FPI-PCIE	2 Series Number 100-Pitch1.00mm	3 Distinction No. 19	4 Type F-Female	5 Circuits XX	6 Entry Angle S-180° Vertical
7 Plating 7-Selective gold plated on contact area and matte tin plated on tails area	8 thickness of Gold Plating 00-Gold Flash 15-15u" 30-30u"	9 Material-Resin 5-PA9T	10 Color-Resin BA-Black HSG,Natural Latch BK-Black HSG,Black Latch BU-Blue HSG, Blue Latch	11 Packaging K-Tray	

Circuits(n)	Part NO.	Dimensions						
		A	B	C	D	E	F	G(REF)
36	FPI10019-F36S7XX5XXK	6.0	7.65	9.15	25.0	9.5	41.55	45.8
64	FPI10019-F64S7XX5XXK	20.0	21.65	23.15	39.0	23.5	55.55	59.8
98	FPI10019-F98S7XX5XXK	37.0	38.65	40.15	56.0	40.5	72.55	76.8
164	FPI10019-F164S7XX5XXK	70.0	71.65	73.15	89.0	73.5	105.55	109.8

 <b>THIRD ANGLE PROJECTION</b> <b>DESIGN UNITS METRIC(mm)</b> <b>SCALE 5:1</b> <b>SIZE A4</b>	<b>GENERAL TOLERANCES (UNLESS SPECIFIED)</b> X. ±0.30    X.' ±5° X.X ±0.20    X.X' ±2° X.XX ±0.15    X.XX' ±1° X.XXX ±0.10    X.XXX' ±0.5°		<b>APPROVE BY</b> LEO <b>CHECKED BY</b> GISELLE <b>DRAWN BY</b> Hejianpeng	<b>DATE</b> 19/Sept/23 <b>DATE</b> 19/Sept/23 <b>DATE</b> 19/Sept/23	<b>PART NO.</b> FPI10019-FXXS7XX5XXK <b>TITLE</b> PCI Express Gen5.0(32GT/S), 180°vertical Pitch 1.0mm SMT <b>THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO TXGA INDUSTRIAL ELECTRONICS(S,Z)CO.,LTD AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION</b>	<b>ITEM NO.</b> FPI10019 <b>REV 0</b> <b>SHEET NO. 1/3</b>	 <b>Building Technology Cornerstone</b>
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A  
B  
C  
D  
E  
F

A  
B  
C  
D  
E  
F

1 2 3 4 5 6 7 8

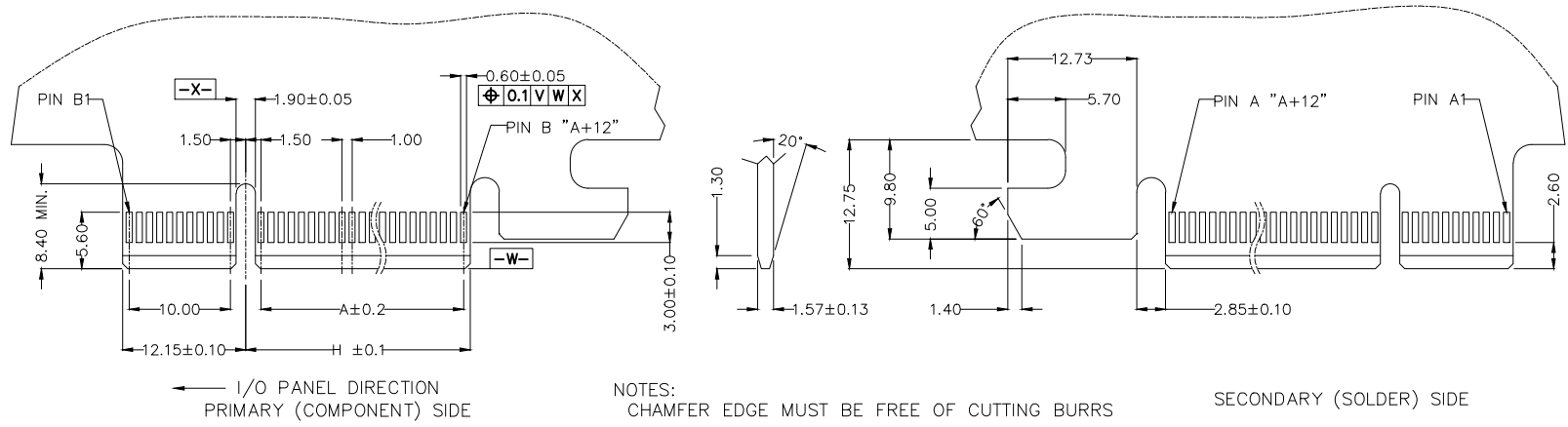
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REV	LOCATIONS	DESCRIPTION	DATE	REVISER	APPD

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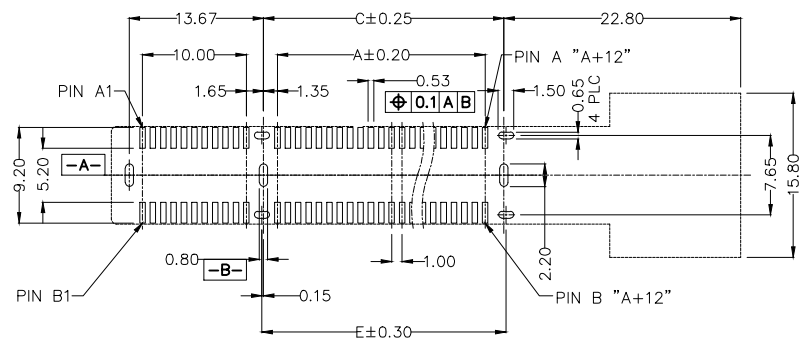
B

C



D

E



Circuits(n)	Part NO.	Dimensions			
		A	H	C	E
36	FPH10019-F36S7XX5XXK	6.0	8.15	9.15	9.5
64	FPH10019-F64S7XX5XXK	20.0	22.15	23.15	23.5
98	FPH10019-F98S7XX5XXK	37.0	39.15	40.15	40.5
164	FPH10019-F164S7XX5XXK	70.0	72.15	73.15	73.5

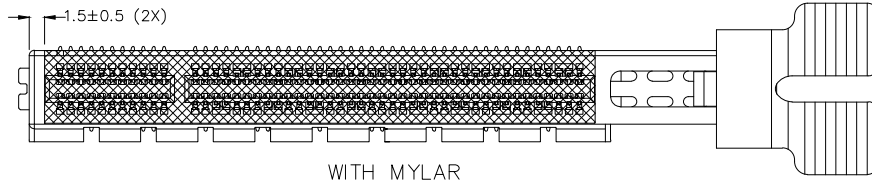
F

<p>THIRD ANGLE PROJECTION</p>	GENERAL TOLERANCES (UNLESS SPECIFIED)		APPROVE BY LEO	DATE 19/Sept/23	PART NO. FPH10019-FXXS7XX5XXK	ITEM NO. FPH10019	<p>Building Technology Cornerstone</p>	
	X. ±0.30	X.' ±5°	CHECKED BY GISELLE	DATE 19/Sept/23	TITLE PCI Express Gen5.0(32GT/S) ,180°vertical Pitch 1.0mm SMT			REV 0
	DESIGN UNITS METRIC(mm)	X.X ±0.20	X.X' ±2°	DRAWN BY Hejianpeng	DATE 19/Sept/23	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO TXGA INDUSTRIAL ELECTRONICS(S,Z)CO.,LTD AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION		SHEET NO. 2/3
	SCALE 5:1	SIZE A4	X.XX ±0.15	X.XX' ±1°	X.XXX ±0.10	X.XXX' ±0.5°		

1 2 3 4 5 6 7 8

REV	LOCATIONS	DESCRIPTION	DATE	REVISER	APPD

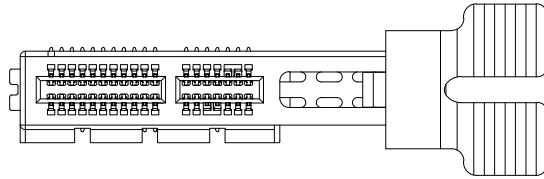
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WITH MYLAR

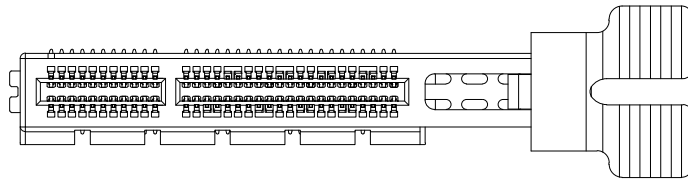
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36 Pos.



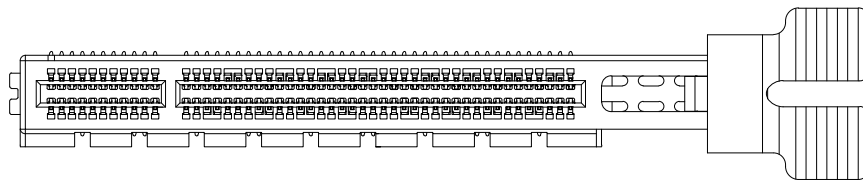
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64 Pos.



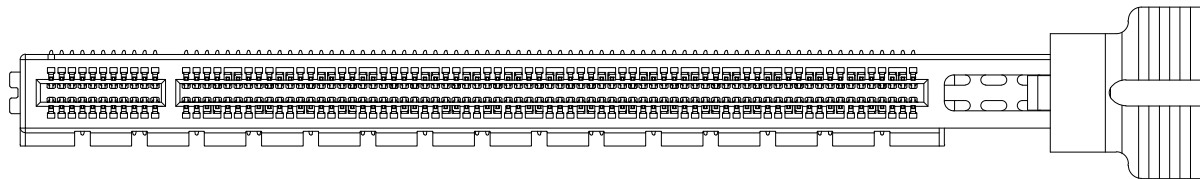
D

98 Pos.



E

164 Pos.



F

<p>THIRD ANGLE PROJECTION</p>	GENERAL TOLERANCES (UNLESS SPECIFIED)		APPROVE BY LEO	DATE 19/Sept/23	PART NO. FPI10019-FXXS7XX5XXK	ITEM NO. FPI10019	<p>Building Technology Cornerstone</p>	
	X. ±0.30	X.' ±5°	CHECKED BY GISELLE	DATE 19/Sept/23	TITLE PCI Express Gen5.0(32GT/S) ,180°vertical Pitch 1.0mm SMT			REV 0
	DESIGN UNITS METRIC(mm)	X.X ±0.20	X.X' ±2°	DRAWN BY Hejianpeng	DATE 19/Sept/23	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO TXGA INDUSTRIAL ELECTRONICS(S,Z)CO.,LTD AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION		
	SCALE 5:1	SIZE A4	X.XX ±0.15 X.XXX ±0.10	X.XX' ±1° X.XXX' ±0.5°				

1 2 3 4 5 6 7 8